Technological Challenges in Sample Prep Operations of High-End Semiconductors at Reverse Engineering

March 19, 2024

REATISS: From Inception to Today

Origin: Initiated 28 years ago, our journey in Reverse Engineering (RE) began with a focus on delivering exclusive services to Motorola, launching our operations from Kyiv, Ukraine.

Expansion: Quickly advancing, we secured our position as an official vendor for Motorola, eventually becoming the primary vendor for Freescale Semiconductor Inc.

Rebranding and Growth: In 2015, we evolved into REATISS, marking our entry into the open market while continuing to expand our expertise. Today, our team consists of nearly 70 dedicated engineers.

Clientele: Our services cater to leading semiconductor manufacturers, patent holders, and intellectual property law firms across the United States and the European Union.

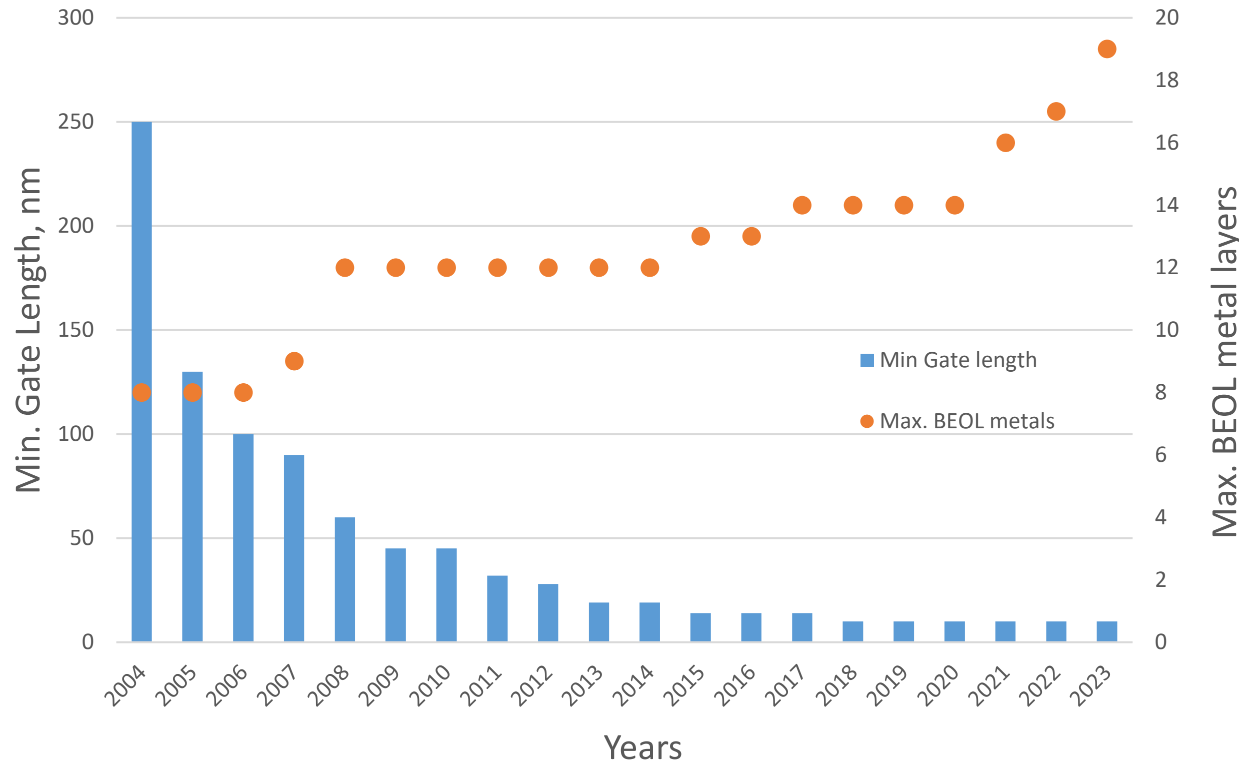
Adaptation and Resilience: Responding to the challenges presented by the full-scale war in Ukraine since 2022, we established an affiliated company in Wroclaw, Poland. This strategic move ensures our ability to continue delivering uninterrupted RE services to our clients, adapting to new circumstances while maintaining our commitment to excellence.

ELENA LESCHUK
Director and CEO

Stages of Reverse Engineering Data Acquisition

- **Sample Preparation:** Preparation of samples is the foundational stage of reverse engineering, demanding advanced techniques to ensure accuracy.
- **Process Analysis:** This involves a thorough examination of the package and die construction, assessing the intricate details of semiconductor devices.
- **Imaging:**
  - **Layer-by-Layer Die Imaging:** Capturing each layer for comprehensive analysis.
  - **Distortion Compensation:** Correcting any image distortions to maintain the integrity of the data.
  - **Stitching:** Combining multiple images to form a complete picture of the semiconductor layout.
- **Synchronization of Digital Maps:** Aligning digital maps of all layers to facilitate seamless navigation, including easy zooming and annotation capabilities.
- **Circuitry Extraction and Analysis:** Deciphering the layout and circuit design details to understand the underlying architecture of the semiconductor device.
- **Patent Claim Mapping:** Developing claim charts that align specific patent claims with the corresponding data obtained from reverse engineering.
- **Interactive Image Database:** Creating a user-friendly database containing 3D high-resolution layout images, complete with a convenient navigation system for efficient data handling.

REATISS Experience



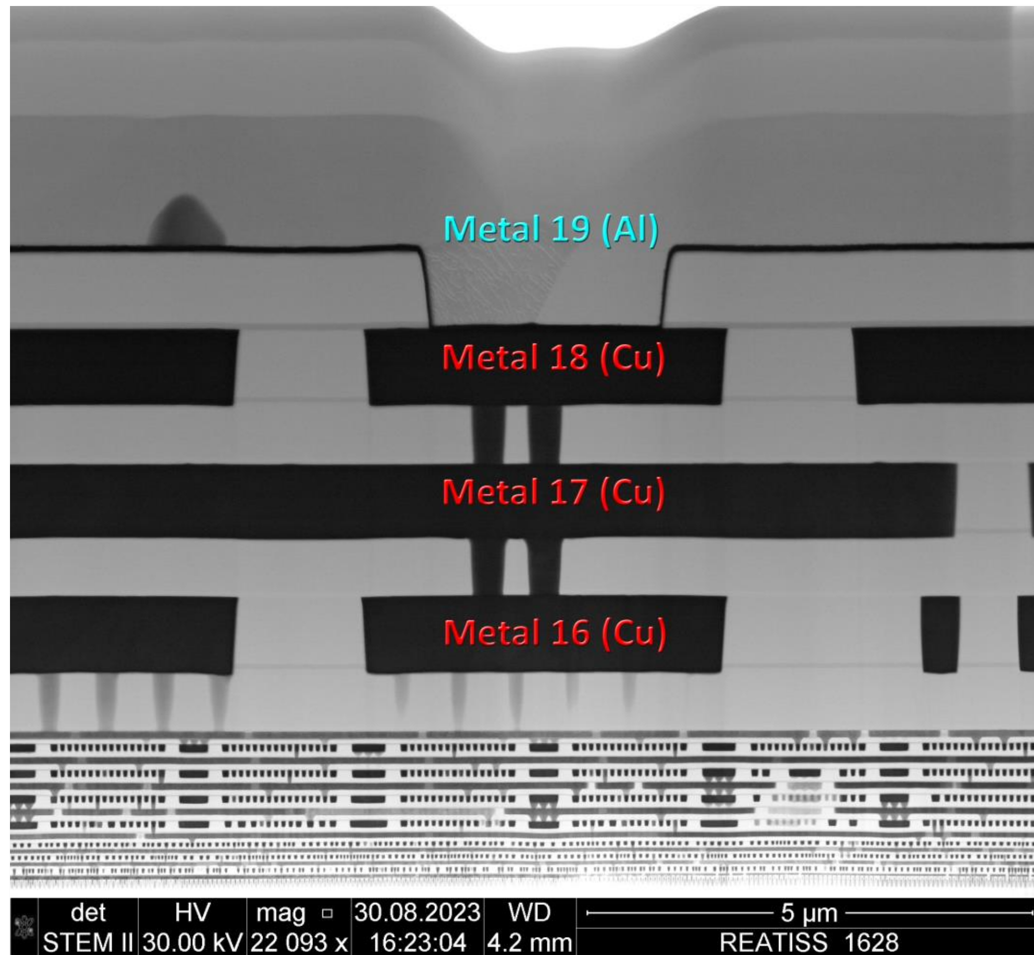
The times of rapid technology scaling are passing by. The smallest nano-features, like minimum gate length, do not change much during last few years.

But the number of metallization layers is constantly increasing, their structure is getting more complex.

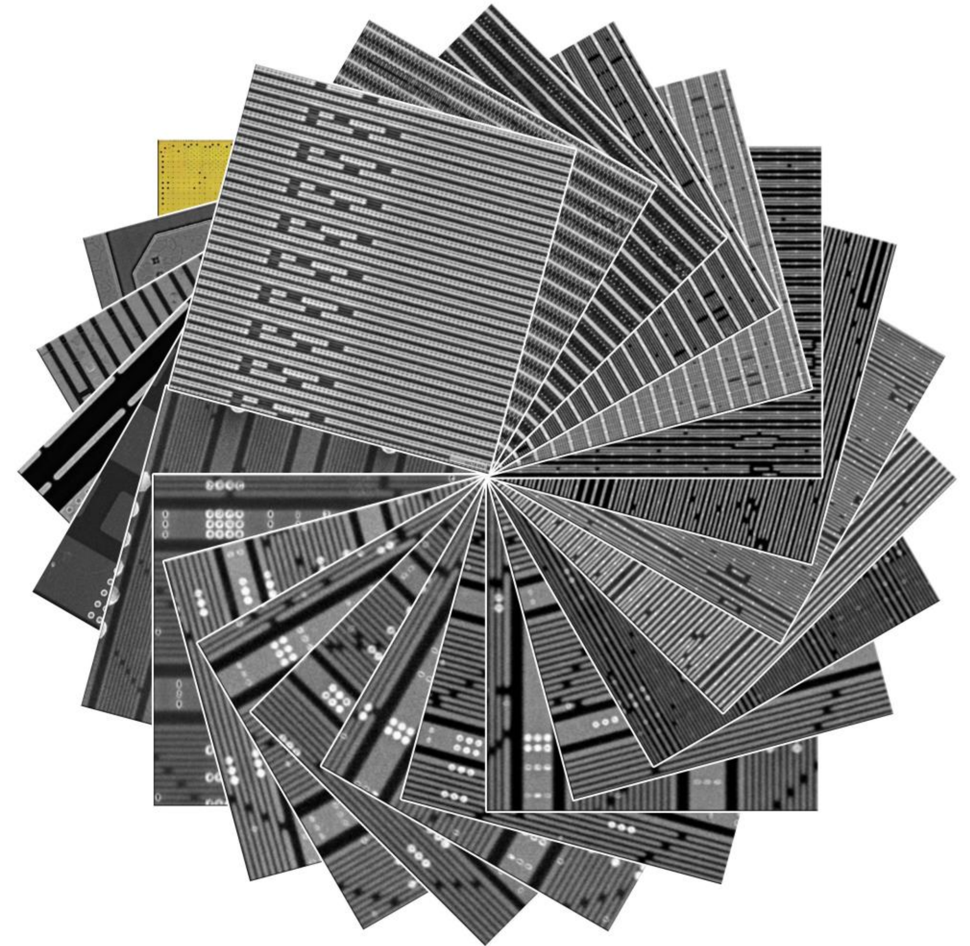
Each new layer brings more complexity to RE analysis and respectively demands more effort.

As for now we are dealing with dice having up to 19 BEOL (Back End of Line) metallization layers.

REATISS Experience with19 Metallization Layers

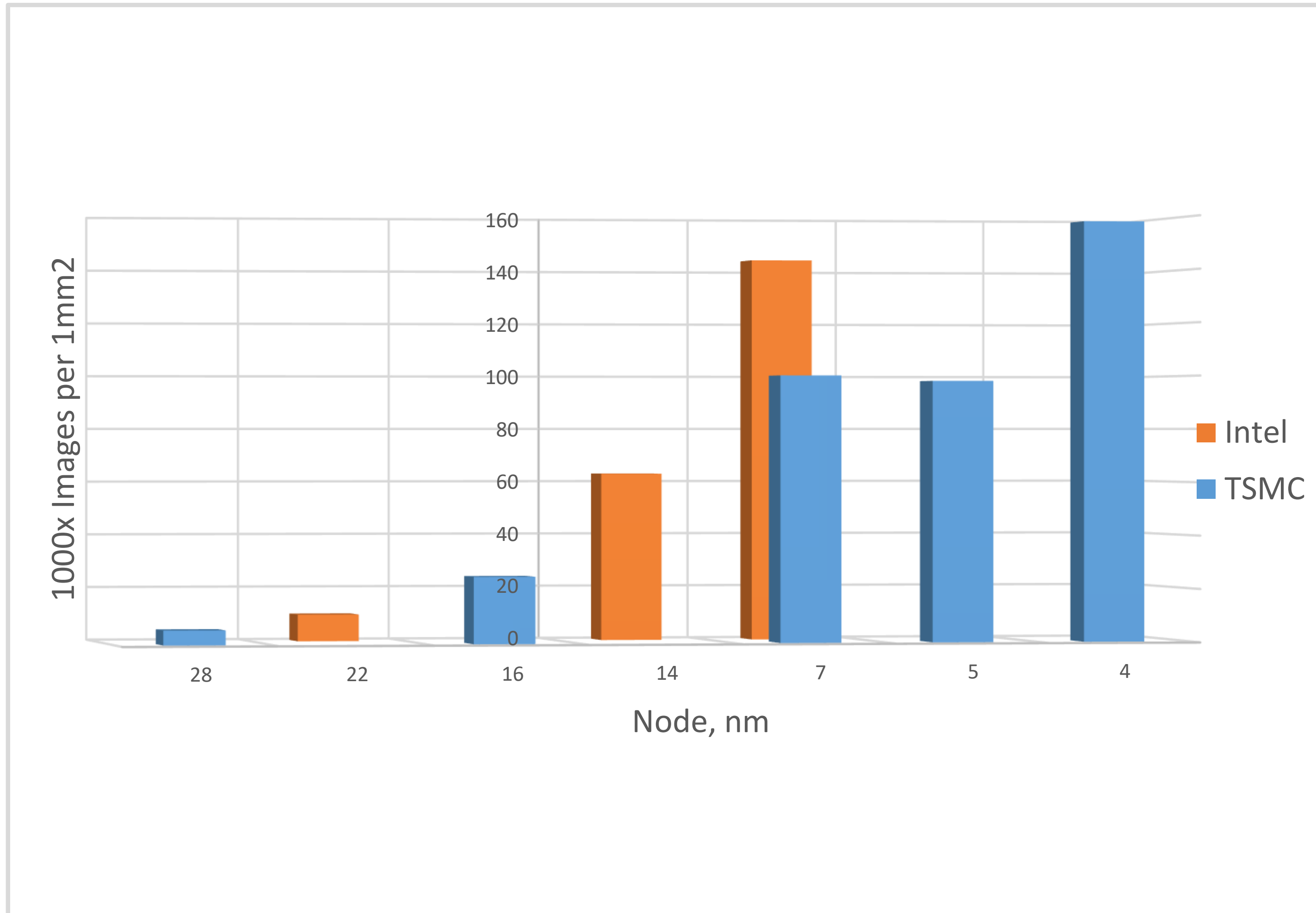


Cross-section of TSMC "N4" technology die with 19 metal layers.



Artistic overview of the prepared and imaged layers.

REATISS Experience – Comparison of Efforts on Intel and TSMC Technologies



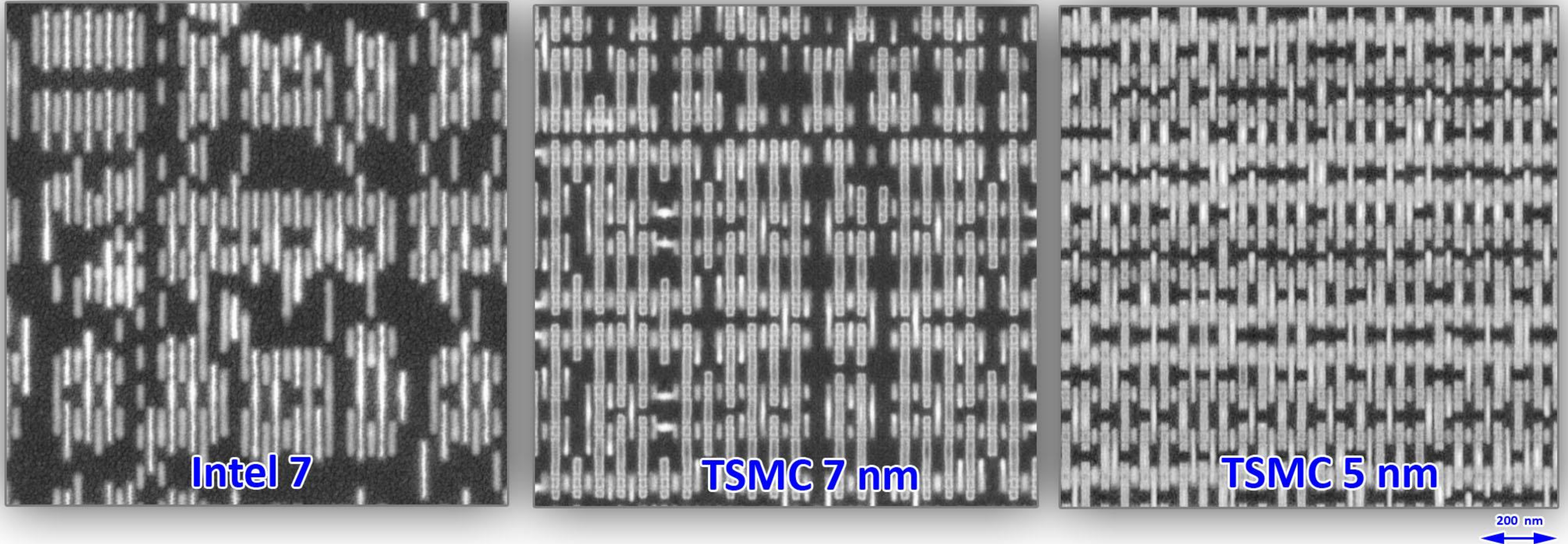
This diagram shows how many images were stitched in average on 1 mm^2 on different technology nodes of such advanced manufacturers as Intel and TSMC.

Noticeable, that Intel 7 technology demands more RE efforts than its closest competing technologies - TSMC 7 nm and TSMC 5 nm.

The reason for that is explained on the following slides.

Comparison of Intel and TSMC Technologies

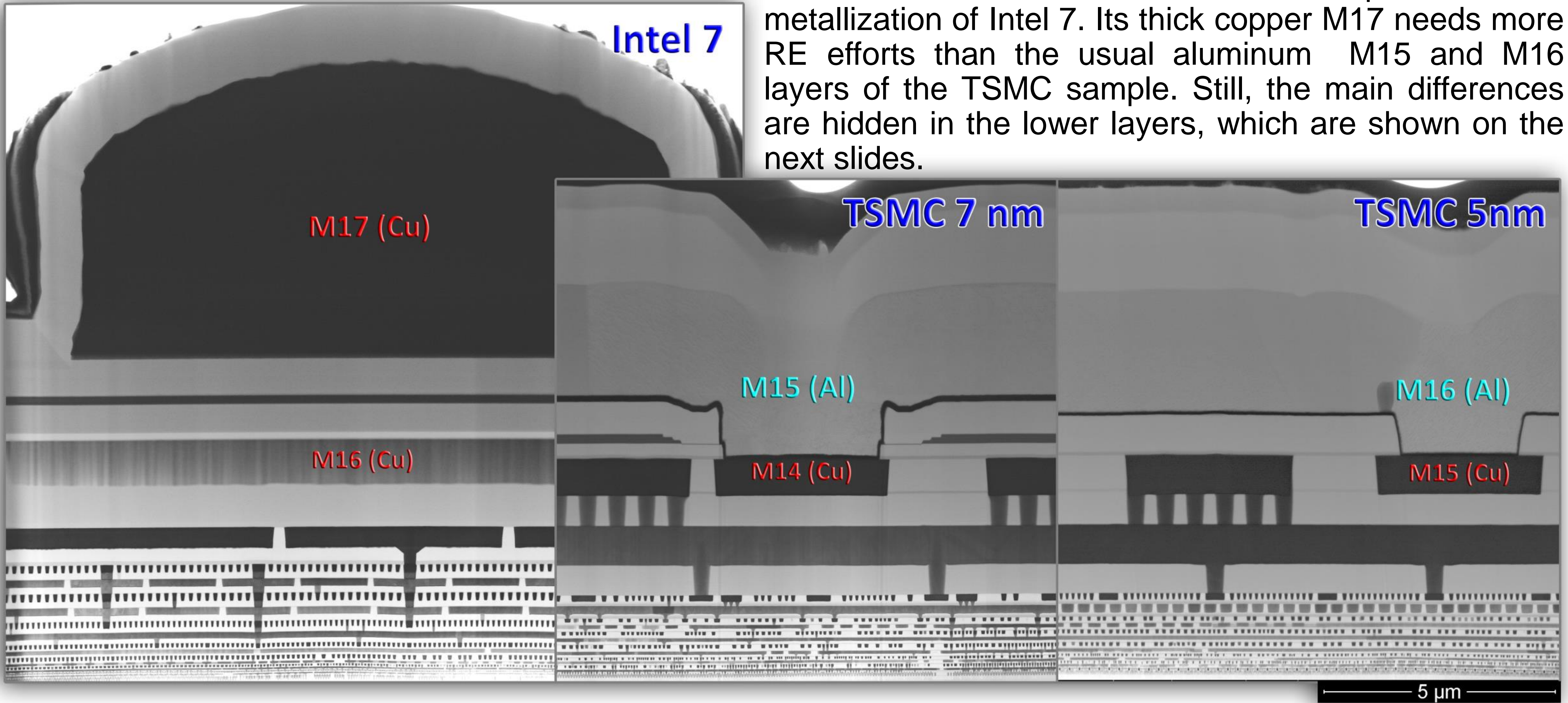
According to technology TSMC 5 nm transistors are packed more densely



Gates layer (logic areas) top views of Intel 7, TSMC 5 nm and TSMC 7 nm samples

Intel vs TSMC

Cross-sections reveal more complex BEOL metallization of Intel 7. Its thick copper M17 needs more RE efforts than the usual aluminum M15 and M16 layers of the TSMC sample. Still, the main differences are hidden in the lower layers, which are shown on the next slides.

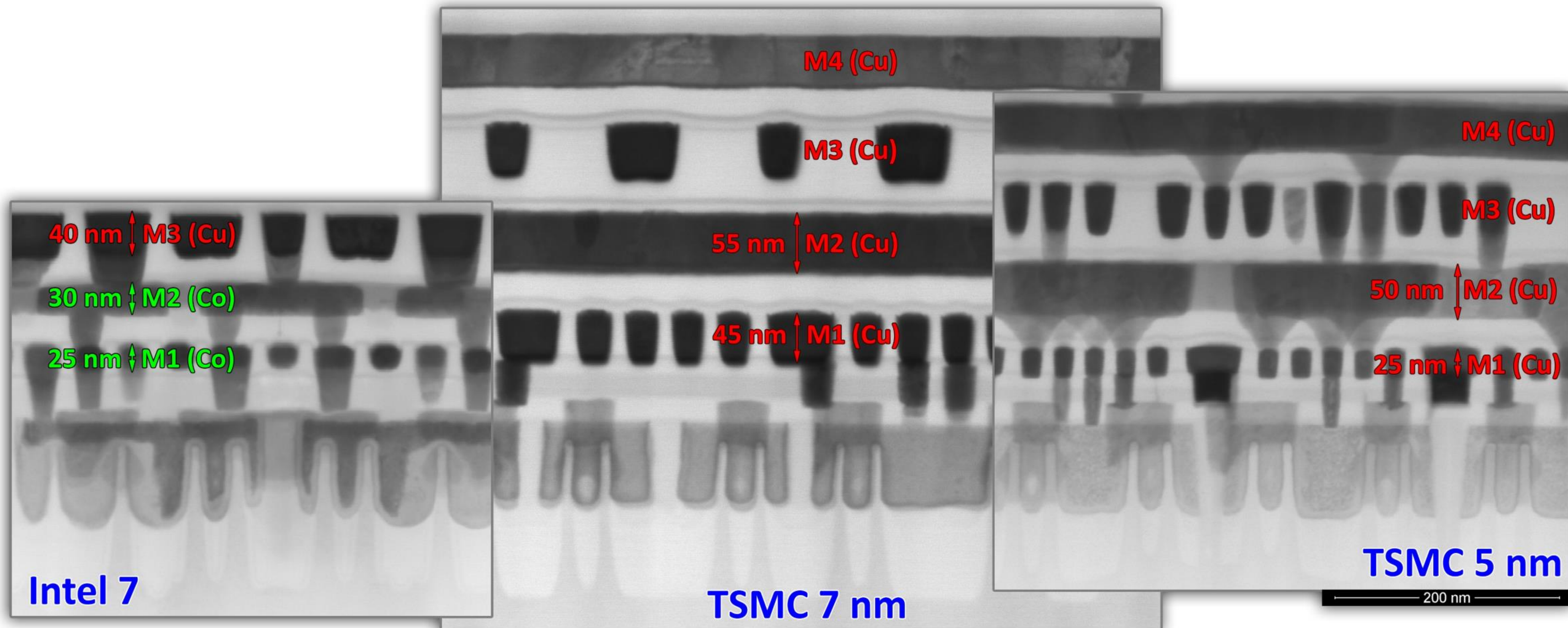


Cross-sections (general views) of Intel 7, TSMC 5 nm and TSMC 7 nm samples

Intel vs TSMC

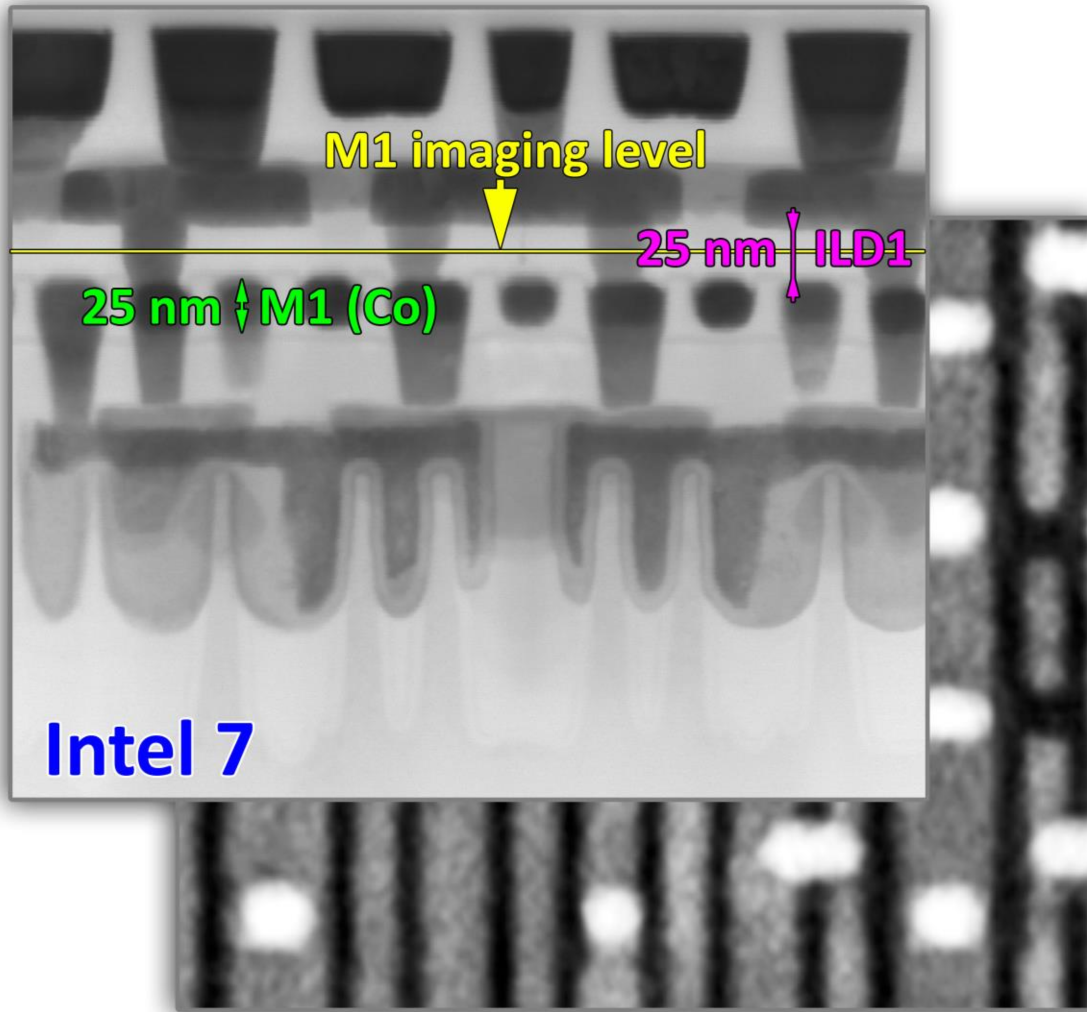
Intel 7 has two noticeable features extremely effort consuming at RE :

- ➢ the thinnest bottom metallization layers;
- ➢ 2 layers of a fragile cobalt metallization



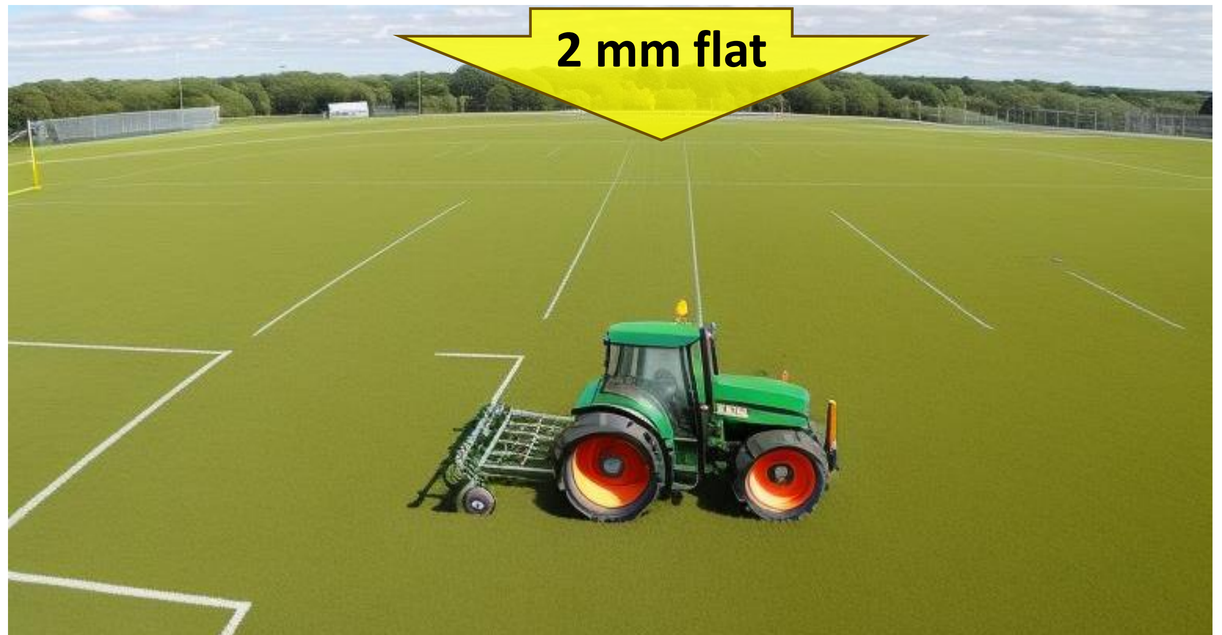
Cross-sections (bottom layers) of Intel 7, TSMC 5 nm and TSMC 7 nm samples

Delayering precision

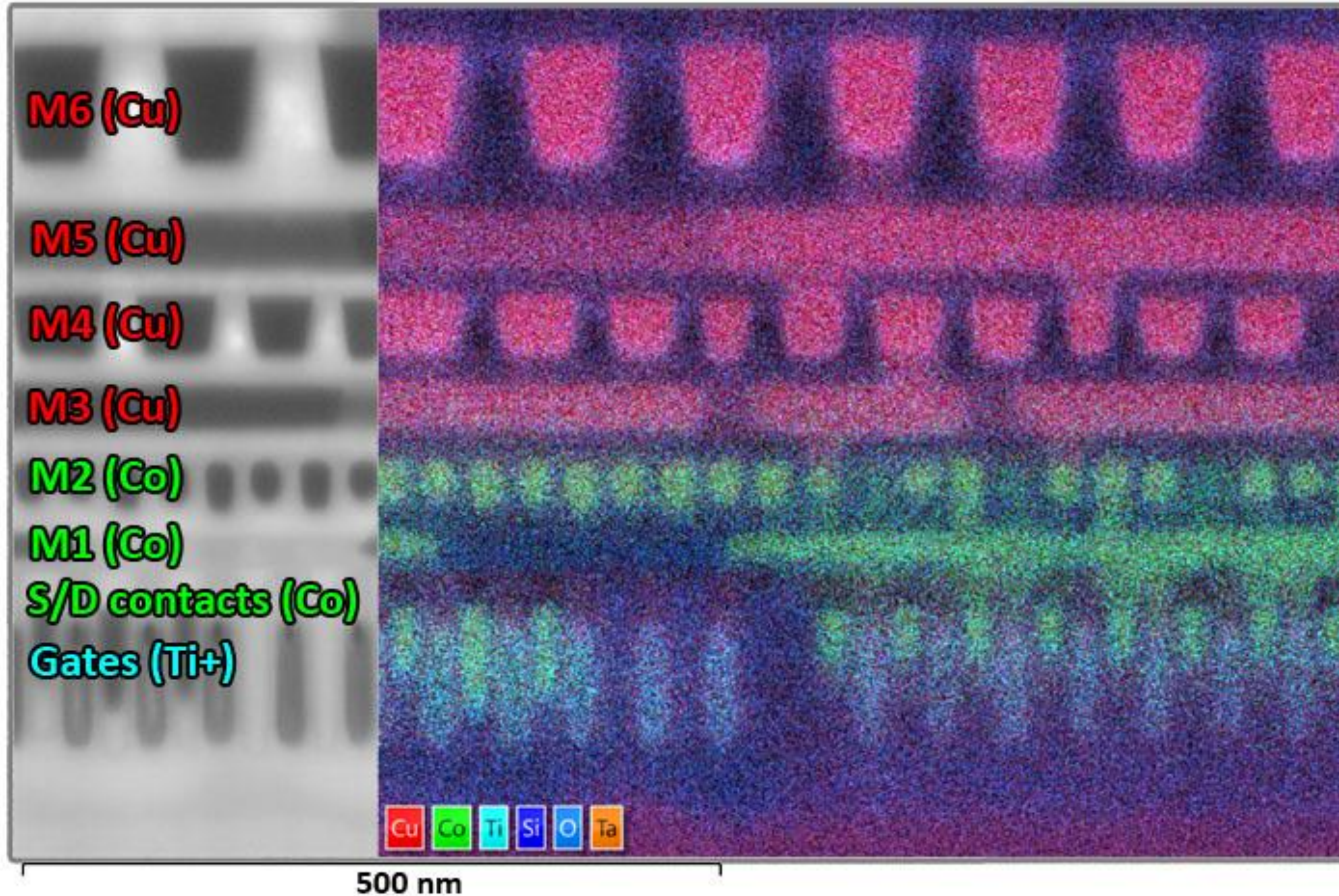


To get successful SEM imaging of M1 layer it is necessary to prepare equal flat surface within 25 nm thickness of ILD1 (Inter Layer Dielectric) across all areas of interest.

Usually, the total area of interest is about 1mm^2 on the die. To understand this situation in macroworld we can illustrate it with a whole football field flattened within 2 mm using a tractor.



Challenging Cobalt Metallization



Intel 7 sample (bottom layers) EDX

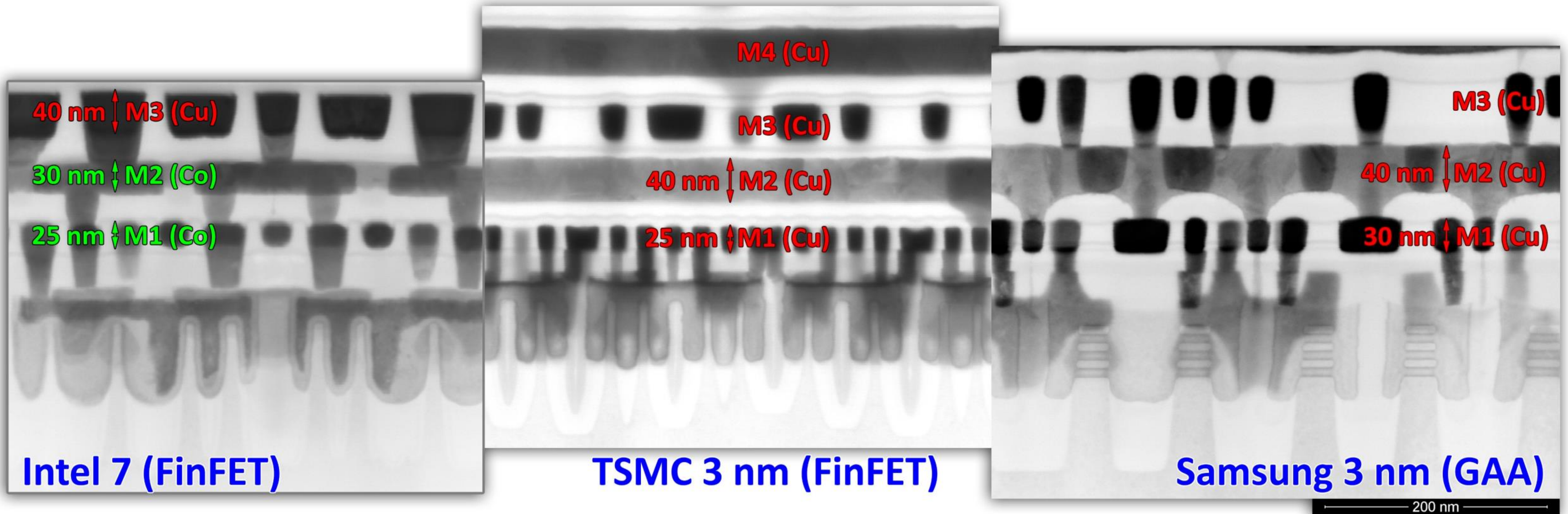
Unlike Al or Cu, the cobalt metallization is very delicate when exposed to air.

It is easily destroyed by water slurries, mild heat, weak acids and bases solutions. This factor greatly limits RE practices applicable to the cobalt layers, demands extra caution and special methods.

So, delayering of the cobalt metallization demands considerably more effort.

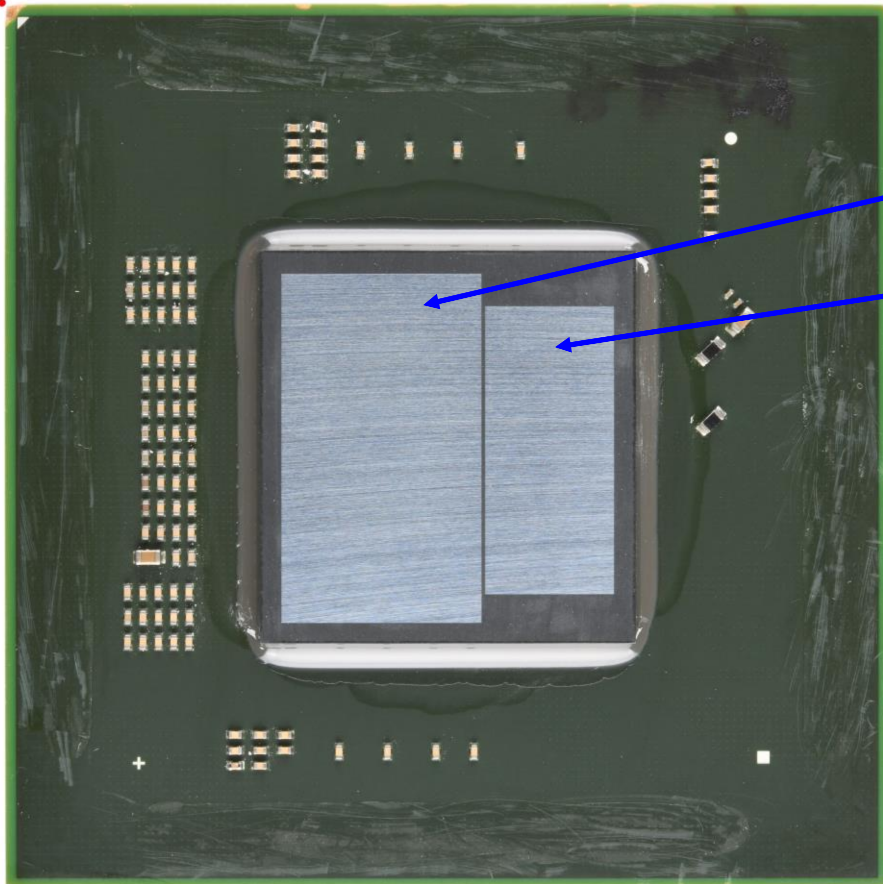
Intel 7 vs the Most High-End Nodes (3nm)

Intel 7 still looks a "Die-Hard" with its thin cobalt metallization

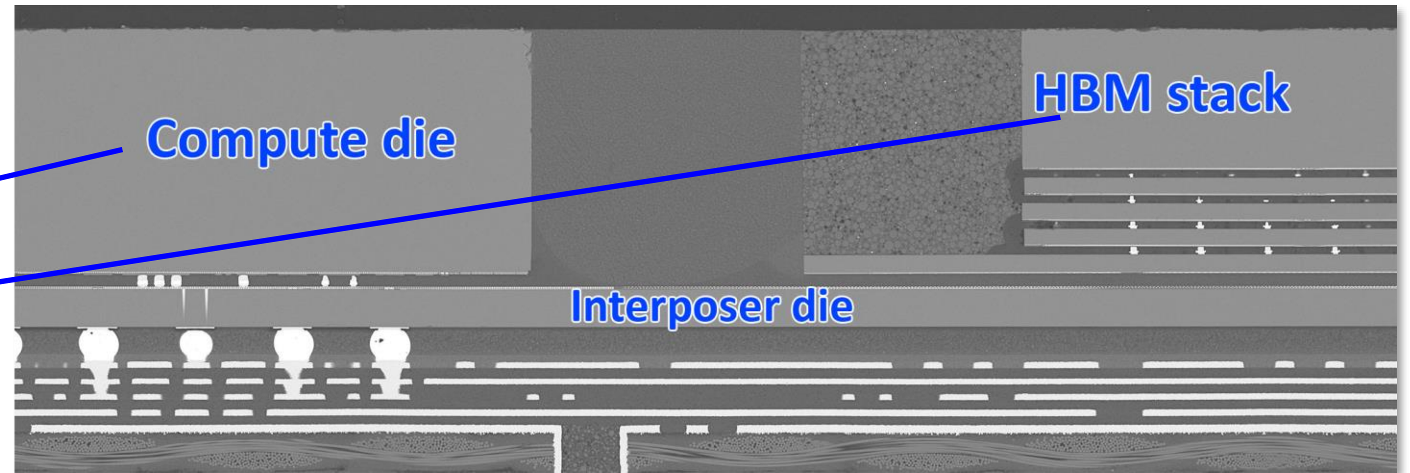


Cross-sections (bottom layers) of Intel 7, TSMC 3 nm and Samsung 3 nm samples

Challenging 3D Packaging



Modern GPU with High Bandwidth Memory



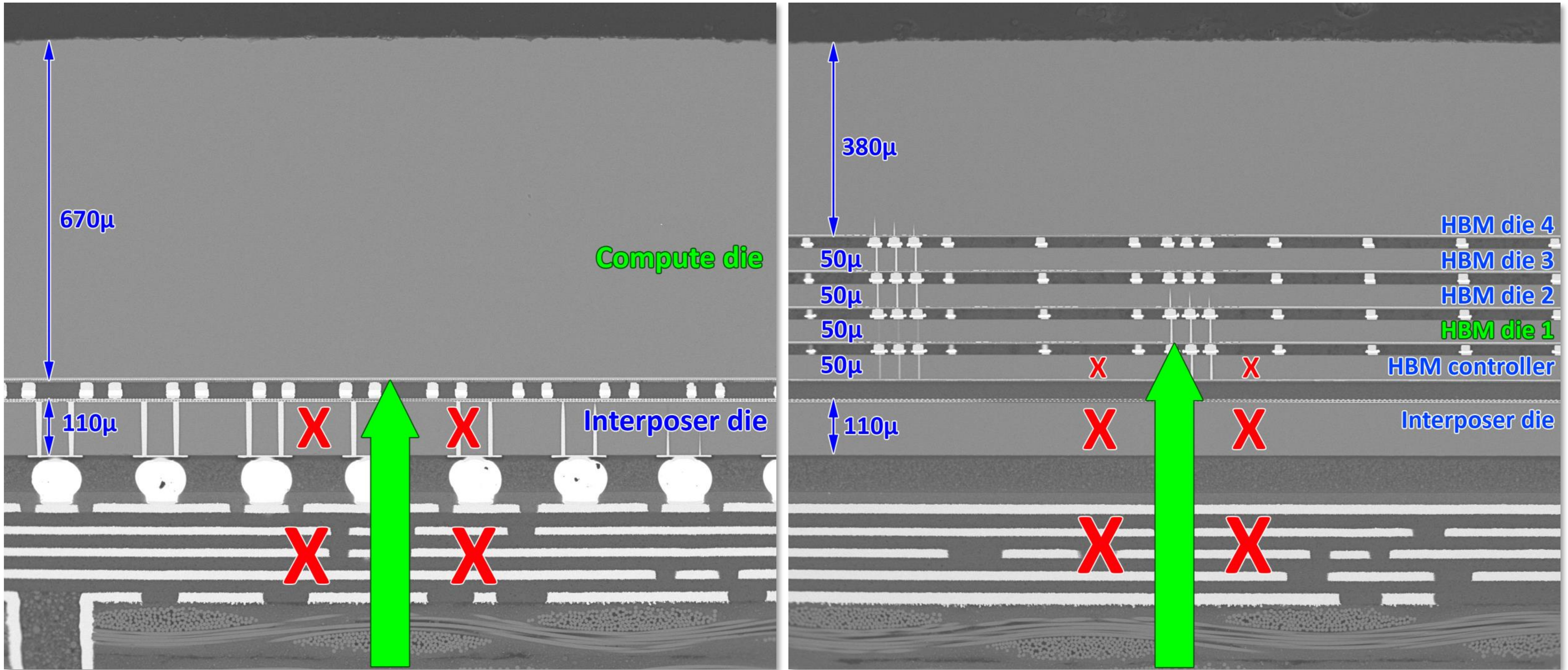
Fragment of a package cross-section of modern GPU with HBM

Complex 3D packaging often does not allow safely extraction of each die.

- Either dice are too firmly connected inside a package
- Or dice are too thin and become so extremely fragile outside a package

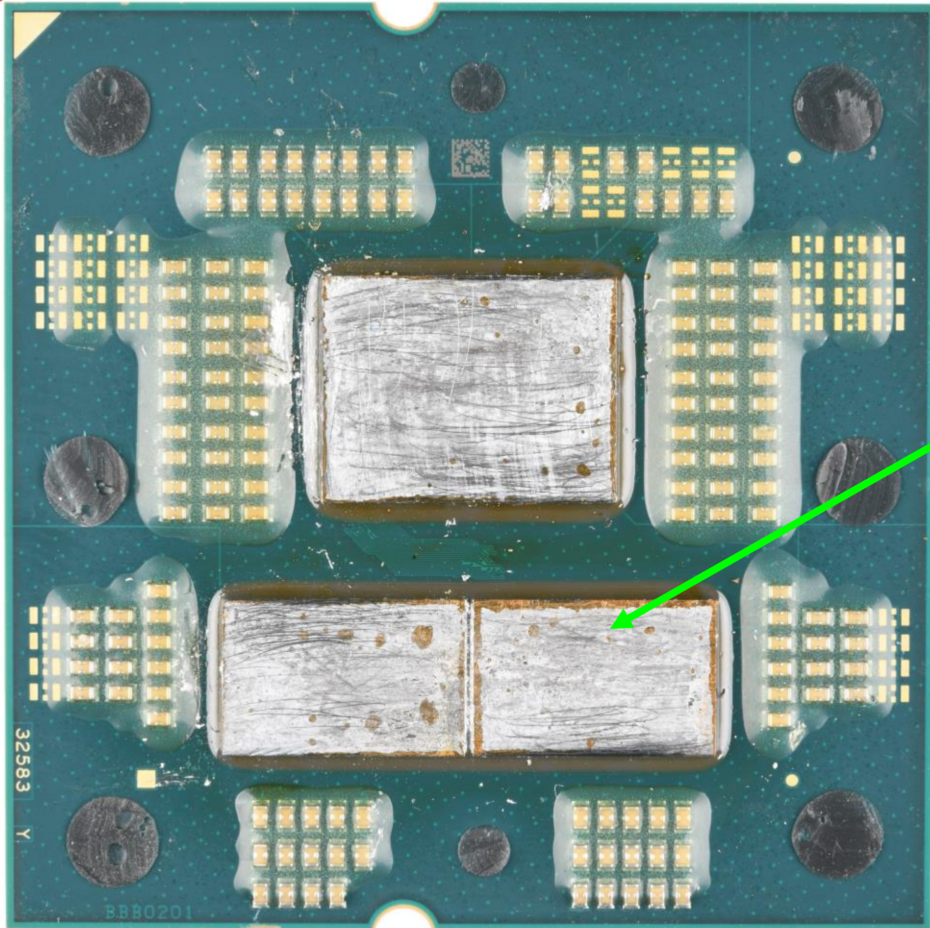
Thus, certain dice need to be sacrificed to reach the other.

Challenging 3D packaging, cont.

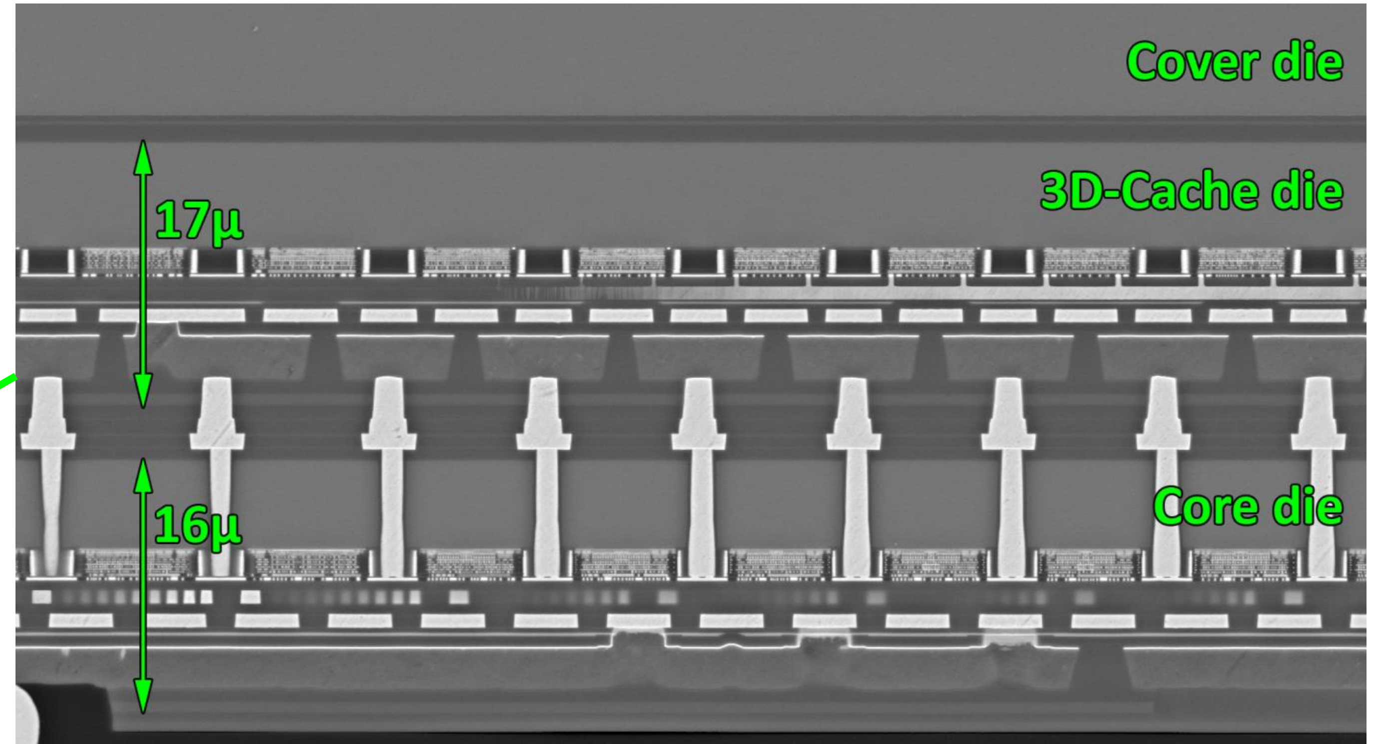


The way to get to a die of interest inside a complex 3D-package

Challenging 3D packaging, cont.



Advanced CPU with 3D-Cache



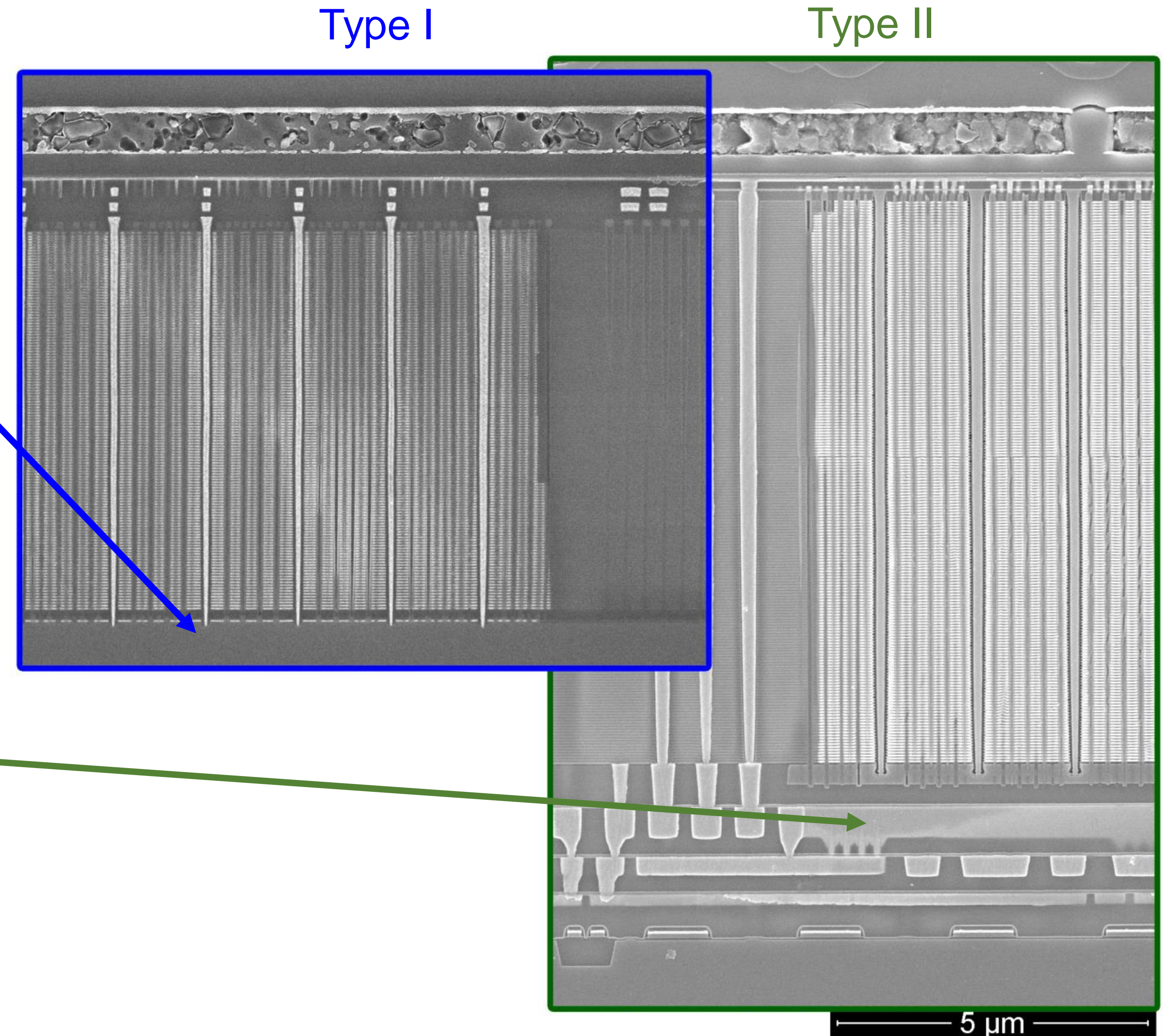
Fragment of a package cross-section of an advanced CPU with 3D-Cache

In this example, the Core die and 3D-Cache die are so thin, that outside of a package they would quickly shatter into pieces.

3D NAND Flash Peculiarities

Type I does not have metallization layers under 3D NAND stack → no reason to worry about the stack delayering → **relatively easy delayering**

Type II on the contrary has metallization layers under 3D NAND stack → the stack must be evenly removed → **very difficult delayering**



3D NAND Flash Peculiarities, cont.

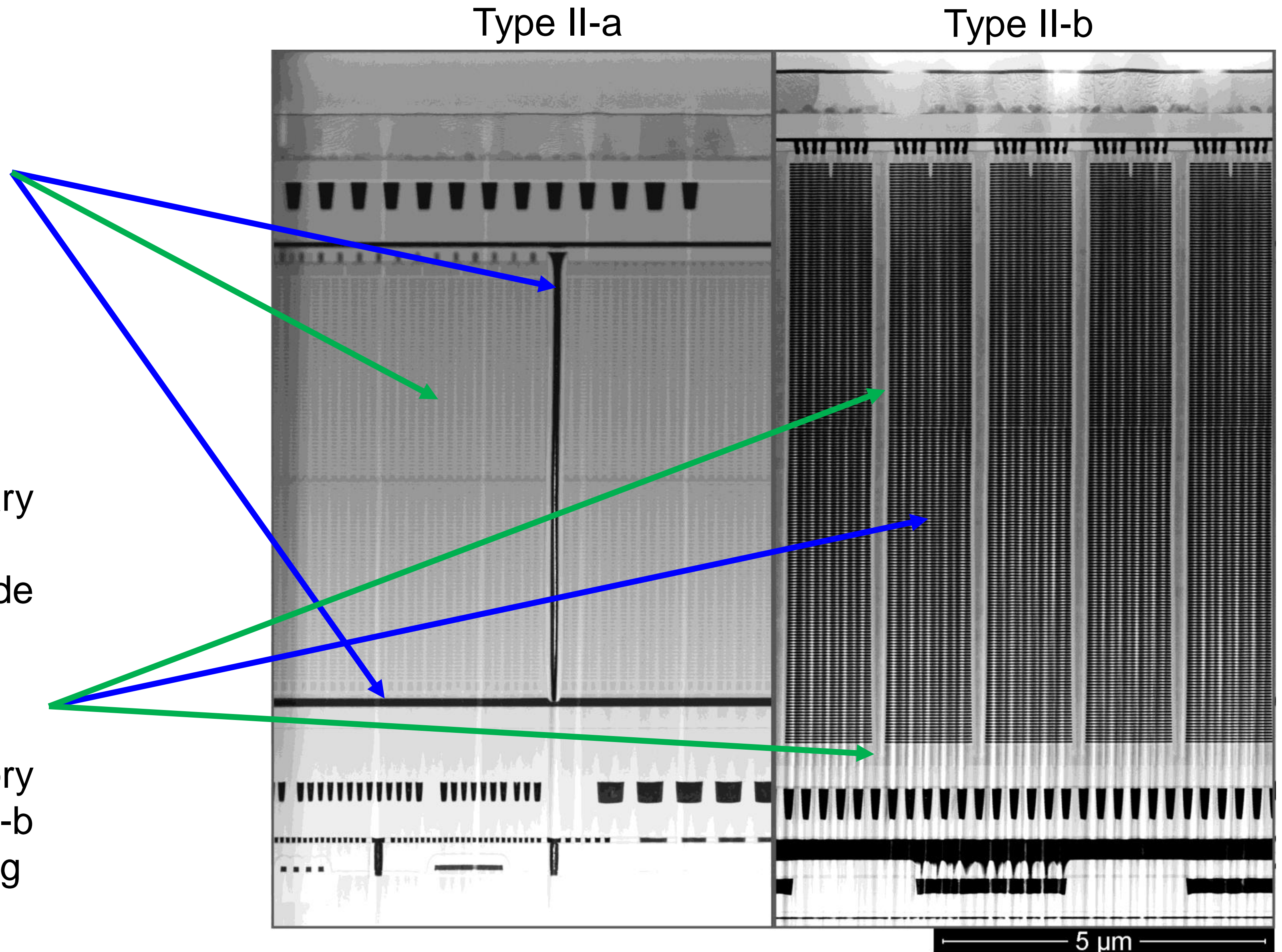
Type II-a contains:

- tungsten common electrode layer and trench vias;
- polysilicon wordlines;

Type II-b on the contrary contains:

- polysilicon common electrode layer and trench vias;
- tungsten wordlines;

Such inversion of the memory stack materials makes type II-b much more difficult for delayering



Samples availability

High-quality RE demands a sufficient number of samples.

For example, Circuit Extraction analysis of high-end devices demands up to 20 samples.

Usually, they are bought separately or found inside modern consumer devices which are available for an affordable price.

But from time to time, we receive requests from customers to perform analysis on very limited number of available samples due to the extremely high price or due to very difficult supply logistics. In this case, the possible realistic scope of analysis also becomes limited.

x 20 =

x 20 =

x 20 =

Conclusions

- With a rapid progress in nanotechnologies, new devices subjected for analysis get more and more complicated. The efforts needed for RE analysis of new-generation devices also go up.
- Some features implemented in certain technologies may significantly increase the difficulty of RE sample preparation and imaging.
- Various devices that are classified as performed with similar technology nodes may actually require noticeably different amounts of effort at RE analysis.
- RE analysis to cover the required scope is possible only if good enough samples are available.

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Thank you
for your attention!