

SAMPLE PREPARATION FOR REVERSE ENGINEERING – CHOOSING THE RIGHT TOOLSET

HARRIS REVERSE ENGINEERING WORKSHOP 2024

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ALLIED HIGH TECH

For over 40 years, Allied High Tech Products has provided the electronic failure analysis community with quality sample preparation products for microscopic evaluation. Allied designs and manufactures a complete line of state-of-the-art sectioning, mounting, milling, grinding & polishing equipment in our California and Oklahoma facilities. Allied's equipment is built in-house to specifications that deliver maximum performance and dependability.



MECHANICAL SAMPLE PREPARATION SOLUTIONS

Mechanical Milling/Grinding/Polishing



X-PREP[®]

Useful for:

Most everything

High Precision

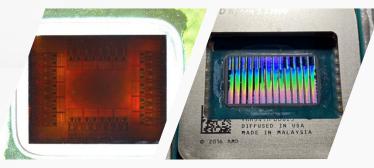


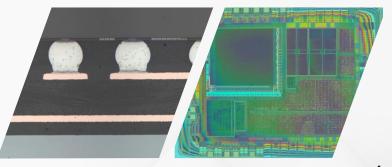
MULTIPREP™

Useful for:

Parallel Delayering

Cross-sectioning





HARRIS 2024

MECHANICAL SAMPLE PREPARATION SOLUTIONS

Mechanical Milling/Grinding/Polishing



TECHCUT 5X[™]

Useful For:

Semi-automated high precision cutting/dicing



TRIMSAW 2X[™]

Useful for:

Manual trimming/component extraction





REVERSE ENGINEERING

- Reverse engineering of semiconductor-based systems is not new/novel and a categorically has been well documented ^[1]:
 - Product teardowns identify the product, package, internal boards, and components
 - System/Component level analysis analyze operations, signal paths, and interconnections
 - Circuit extraction delayer to transistor level, then extract interconnections and components to create schematics
 - Process analysis examine the structure and materials to see how it is manufactured

> BUT WHAT TOOLSET SHOULD BE USED?





PRODUCT TEARDOWNS

- Product teardowns can be simple, provided the system boards/ components are easy to access.
 - □ Toolsets might consist of the following:
 - Screwdrivers
 - o Tweezers
 - Scalpel/Razor blades
- Once exposed the boards and subassemblies can be photographed.

> WHAT IF PACKAGE CANNOT "BROKEN INTO" WITHOUT RISK OF BRUTE FORCE DAMAGE?

PRODUCT TEARDOWNS

Sometimes the package is not easily opened. \rightarrow Toolset X-Prep



"BREAKING IN"

Mounting the part and leveling to make sure milling tool is perpendicular to cutting plane.

REDUCE RISK OF THERMAL DAMAGE

Matching the milling tool to the material being removed will allow for dry cutting without increased temperature risk.

PRECISION REMOVAL

External package removed, board/component can be extracted.

PHOTO DOCUMENTATION

Board removed and remounted for additional analysis/selective deconstruction.

PRODUCT TEARDOWNS

Carefully deconstruct the device to expose all components \rightarrow Toolset X-Prep



SELECTIVE AREA DECONSTRUCTION

Utilizing a CNC based machine the sample is mounted for selective deconstruction.

REMOVAL OF SHIELDING

REPAIRWZEXH

SLQ6120AA F14/110505/N/490

Record part/component markings, even include non specific labels.

PRECISION REMOVAL

End mill used to remove the shield (dry cut) while still preserving all circuitry/components under shield.

PHOTO DOCUMENTATION

After shield is removed and device cleaned-up photo documentation can resume.



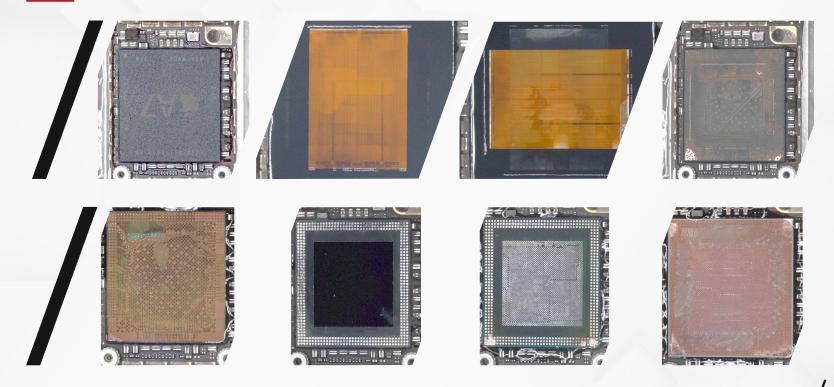


SYSTEM/COMPONENT LEVEL ANALYSIS

- Reverse engineering whether system level or component level is hierarchical analysis method.
 - Photo documentation and electrical analysis must be considered when selectively deconstructing.
 - Layer-by-layer analysis requires precision techniques and is not for the feint of heart.
 - Knowledge of the component is critical when deconstructing
 - Assistance of X-Ray and/or device crosssection is helpful

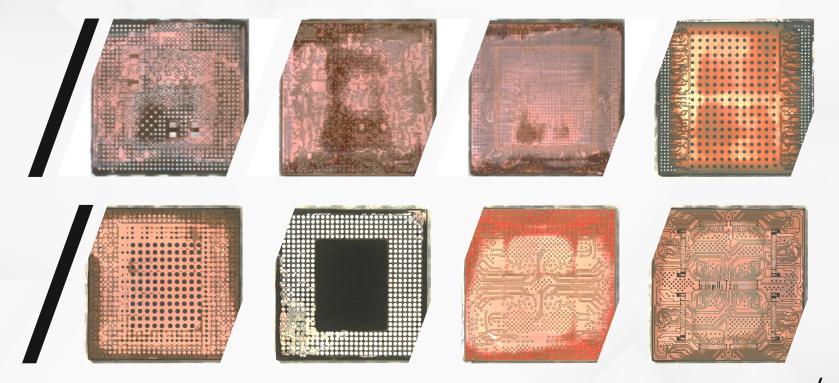
SYSTEM/COMPONENT LEVEL ANALYSIS

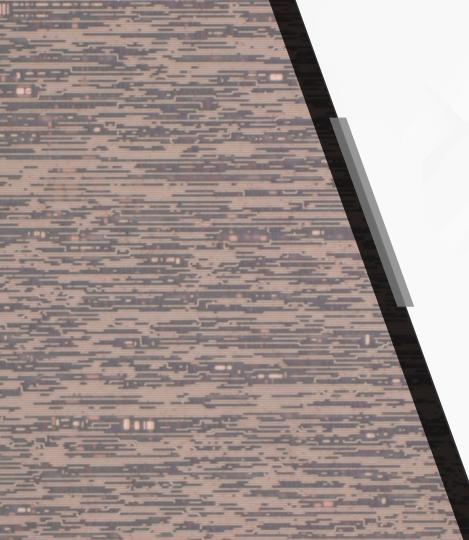
Component level deconstruction (not all layers shown) → Toolset X-Prep



SYSTEM/COMPONENT LEVEL ANALYSIS

PCB Layer-by-Layer Analysis \rightarrow Toolset X-Prep



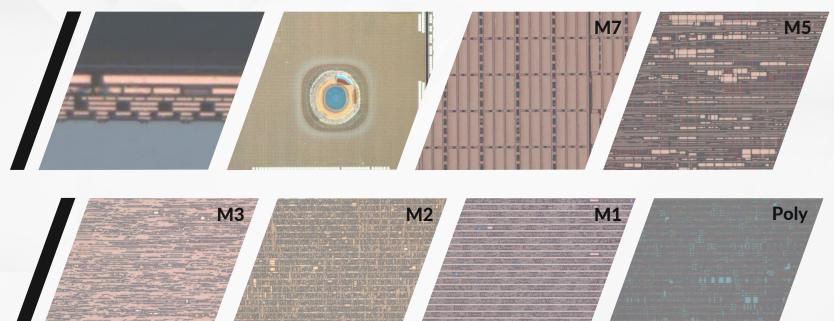


CIRCUIT EXTRACTION

- Circuit extraction can be the most challenging as it might require a combination of methods such as mechanical polishing, plasma (dry) etching and wet etching.
- It is additionally complicated by technology size, metallization (Cu/Al and combinations), circuitry density, number of layers, etc.
 - Cross-sections can be helpful in obtaining this information.
- The challenge, should you choose to accept it, is edge-to-edge uniform deprocessing to allow for:
 - □ Imaging
 - Annotation
 - □ Schematic read-back
 - Analysis

CIRCUIT EXTRACTION

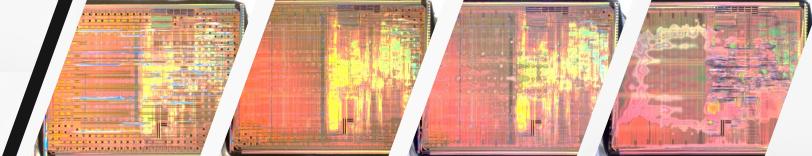
Area specific 2 mm x 2 mm region \rightarrow Toolset X-Prep

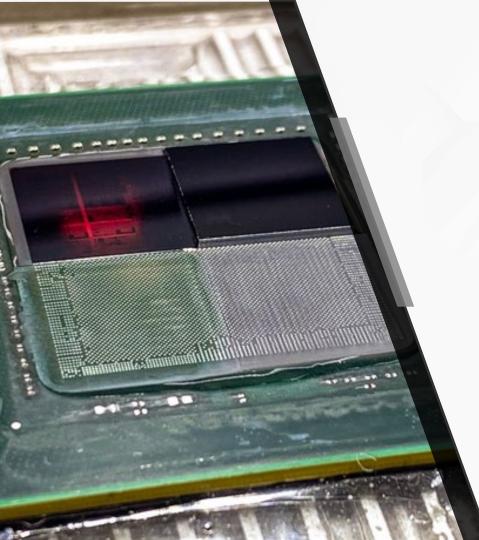


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CIRCUIT EXTRACTION

Edge-to-Edge extracted from ceramic package – Top 3 thick metal layers removed \rightarrow Toolset X-Prep \rightarrow Once extracted, Toolset MultiPrep





PROCESS ANALYSIS

- Process analysis of chips can entail a deep dive into a specific area of a chip which requires specific/precise deconstruction.
- Advanced packaging technology and heterogeneous packaging present different challenges when trying to keep the device electrically intact.

PROCESS ANALYSIS

Complex Heterogeneous packages may require different devices be analyzed. → Toolset X-Prep



HETEROGENEOUS PACKAGES

Removing top two of three memory chips in a stacked configuration

REMOVING SILICON TO EXPOSE CIRCUIT

Targeted thinning and polishing, just removed a silicon

THINNING TO SUB 5 MICRON

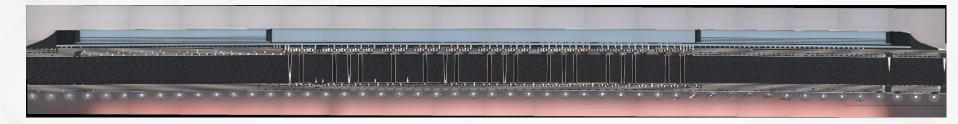
SOC thinned between HMB structures to allow for biased analysis

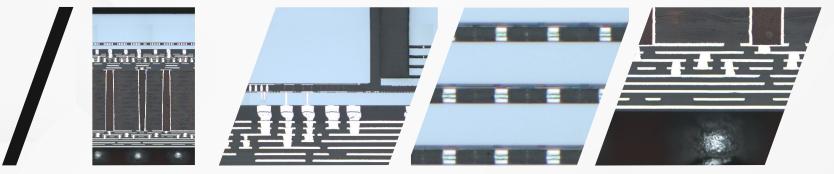
INTERPOSER INSPECTION

Top HBM removed to expose interposer between die

PROCESS ANALYSIS

Cross-sectioning of large device is best done mechanically – High Resolution auto stitched \rightarrow Toolset MultiPrep

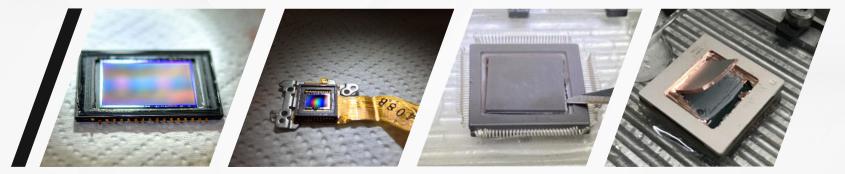






- Reverse engineering isn't always global, sometimes it can be very specific to a region
- Additional examples Time Permitting

Complex Heterogeneous packages may require different chiplets be analyzed. → Toolset X-Prep



SENSORS

Removing the glass cover, without damage to the device

SENSOR ON FELX

Removing the glass cover, without damage to the device

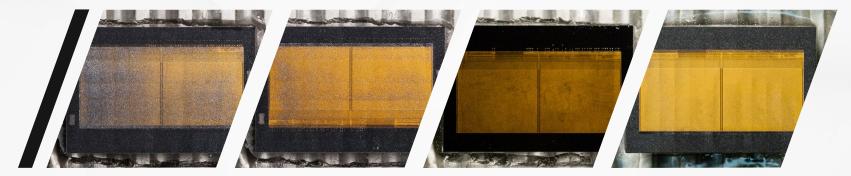
CERAMIC

Removing ceramic lid without flooding cavity or damaging bondwires.

HEAT SPREADER

Easily Remove heat spreader leaving bulk of deice at full package thickness

Stacked Memory Die (8 devices)→ Toolset X-Prep



TOP DIE

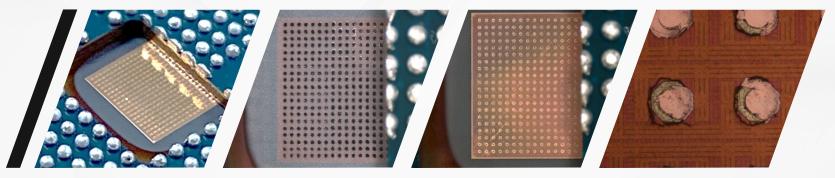
DIE 2

DIE 3

DIE 4

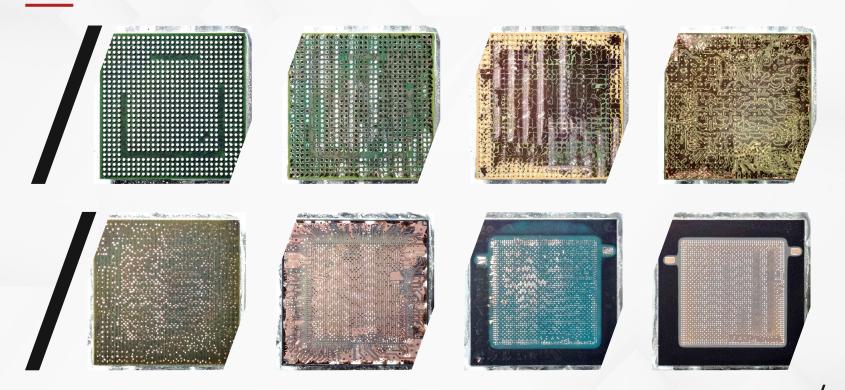
Die were removed in order to expose the 4th die in the stack. Stopping just above Die 4 DAF that can be removed chemically or with atmospheric plasma

Selective exposure of Cu Pillars 6 mm x 4 mm window \rightarrow Toolset X-Prep



FINISHED DEVICE APPROACHING DIE 5 MICRONS 500X IMAGE SURFACE

PCB Layer-by-Layer Analysis \rightarrow Toolset X-Prep



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THANK YOU

QUESTIONS?

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